AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions:

1. (Currently Amended) A processor comprising:

a first port to receive a plurality of supply voltages from at least one ~~supply voltage from an~~ external voltage regulator, each of the plurality of supply voltages ~~the supply voltage~~ to power a particular portion of the processor;

a plurality of voltage sensors, each of the plurality of voltage sensors to monitor one of the plurality of supply voltages ~~voltage sensor to monitor the supply voltage~~; and

a second port to provide a plurality of control signals from the plurality of voltage sensors ~~control signal from the voltage sensor~~ to the at least one voltage regulator, each of the plurality of control signals to indicate if ~~the~~ a respective supply voltage is above or below a target value corresponding to a respective portion of the processor, ~~wherein the target value is to be reduced if the circuit is inactive~~.

2. (Currently Amended) The processor of claim 1, wherein at least one of the target values ~~the target value~~ is adjustable by the processor in accordance with a power management policy.

3. (Currently Amended) The processor of claim 1, wherein at least one of the target values ~~the target value~~ is to be set to allow the processor to meet a timing requirement.

4. (Canceled)

5. (Currently Amended) The processor of claim 1, wherein at least one of the voltage sensors ~~the voltage sensor~~ includes an op amp.

6. (Currently Amended) The processor of claim 1, wherein ~~the circuit includes at least a portion of~~ a core of the processor comprises one of the portions of the processor to be powered by one of the plurality of supply voltages.

7. (Currently Amended) The processor of claim 1, wherein ~~the circuit includes~~ a memory region of the processor comprises one of the portions of the processor to be powered by one of the plurality of supply voltages.

8. (Currently Amended) The processor of claim 7, wherein the memory region is a cache.

9. (Currently Amended) A computer system comprising:

a discrete voltage regulator to provide a plurality of supply voltages ~~supply voltage~~; and

a processor, powered by the plurality of supply voltages ~~supply voltage~~, to provide a plurality of control signals ~~control signal~~ to the voltage regulator, each of the plurality of control signals to indicate if a respective supply voltage is above or below a target value corresponding to a respective portion of the processor powered by the respective supply voltage ~~a target value for the supply voltage, wherein the target value is to be reduced if at least a portion of the processor is inactive~~.

10. (Currently Amended) The computer system of claim 9, wherein at least one of the target values ~~the target value~~ is to be adjusted by the processor in accordance with a power management policy.

11. (Currently Amended) The computer system of claim 9, wherein at least one of the target values ~~the target value~~ is to be set to allow the processor to meet a timing requirement.

12. (Canceled)

13. (Currently Amended) The computer system of claim 9, wherein at least one of a core of the processor or a memory region of the processor comprise portions of the processor to be powered by the plurality of supply voltages ~~the target value is to be indicated by the control signal by indicating if the supply voltage is above or below the target value~~.

14. (Currently Amended) The computer system of claim 9, wherein the processor includes a plurality of voltage sensors ~~voltage sensor~~ to monitor the ~~supply voltage~~ plurality of supply voltages and to provide the plurality of control signals ~~control signal, the voltage sensor including an op amp~~.

15. (Currently Amended) A method comprising:

enabling a voltage regulator to provide ~~Vcc~~ a plurality of supply voltages to a processor;

enabling the processor to receive ~~Vcc~~ the plurality of supply voltages from the voltage regulator and to send a plurality of control signals ~~control signal~~ associated with ~~Vcc~~ the plurality of supply voltages to the voltage regulator, each of the plurality of control signals ~~the control signal~~ to indicate if a respective supply voltage is above or below a target value corresponding to a respective portion of the processor powered by the respective supply voltage ~~a target value~~; and

enabling the voltage regulator to receive the plurality of control signals ~~control signal~~ from the processor, the voltage regulator to adjust ~~Vcc~~ the plurality of supply voltages to the respective target values ~~target value~~ in response to the plurality of control signals ~~control signal; and~~

~~reducing the target value if at least a portion of the processor is inactive~~.

16. (Currently Amended) The method of claim 15, wherein enabling the voltage regulator to provide ~~Vcc~~ the plurality of supply voltages to the processor includes electrically coupling a ~~Vcc~~ voltage supply output of the voltage regulator to a ~~Vcc~~ voltage supply input of the processor.

17. (Currently Amended) The method of claim 15, wherein enabling the voltage regulator to receive the plurality of control signals ~~control signal~~ from the processor includes electrically coupling a ~~Vcc~~ voltage supply control output of the processor to a ~~Vcc~~ voltage supply control input of the voltage regulator.

18. (Canceled)

19. (New) The processor of claim 1, wherein at least one of the target values is to be reduced if a corresponding portion of the processor is inactive.

20. (New) The computer system of claim 9, wherein at least one of the target values is to be reduced if a corresponding portion of the processor is inactive.

21. (New) The method of claim 15 further comprising:

reducing at least one of the target values if a corresponding portion of the processor is inactive.